

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Michael H. Perrott, Rex T. Baird, Yunteng Huang

Title: DIGITALLY-SYNTHESIZED LOOP FILTER CIRCUIT
PARTICULARLY USEFUL FOR A PHASE LOCKED LOOP

Application No.: Not Yet Assigned Filed: Herewith

Examiner: Not Yet Assigned Group Art Unit: Not Yet Assigned

Atty. Docket No.: 026-0002-1

September 5, 2003

Mail Stop Patent Application
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**INFORMATION DISCLOSURE STATEMENT
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Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings the patents, publications, applications or other information identified in the attached:

- Form(s) PTO-1449
- Copy of International Search Report for PCT/US01/21645
- Copy of International Search Report for PCT/US01/21644

to the Examiner's attention in the above-identified application. These references were cited in parent Application No. 09/902,541, filed July 10, 2001. Accordingly, in accordance with C.F.R. §1.98(d), copies of references are not being supplied herewith. Citation of such information shall not be construed as:

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For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

FEE AUTHORIZATION

- This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
- The undersigned believes that this Information Disclosure Statement is being filed before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.

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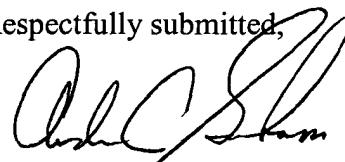
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Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office		Attorney Docket No.: 026-0002-1
		Application No.: <i>Not Yet Assigned</i>
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s): <i>Michael Perrott et al.</i>
(Use several sheets if necessary)		Filing Date: <i>Herewith</i>
		Group Art Unit: <i>Not Yet Assigned</i>
		Date Submitted: <i>September 5, 2003</i>

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name
	AA	6,150,891	Nov. 21, 2000	Welland et al.
	AB	6,167,245	Dec. 26, 2000	Welland et al.
	AC	6,147,567	Nov. 14, 2000	Welland et al.
	AD	6,137,372	Oct. 24, 2000	Welland et al.
	AE	6,075,416	Jun. 13, 2000	Dalmia
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	AG	6,008,703	Dec. 28, 1999	Perrott et al.
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					Translation	
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	AR	Andersson, L. I. et al., "Silicon Bipolar Chipset for SONET/SDH 10 Gb/s Fiber-Optic Communication Links," IEEE Journal of Solid-State Circuits, Vol. 30, No. 3, Mar. 1995, pp. 210-218.
	AS	Belot, D. et al., "A 3.3-V Power Adaptive 1244/622/155 Mbit/s Transceiver for ATM, SONET/SDH," IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, Jul. 1998, pp. 1047-1058.
	AT	Gray, C. T. et al., "A Sampling Technique and Its CMOS Implementation with 1 Gb/s Bandwidth and 25 ps Resolution," IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, Mar. 1994, pp. 340-349.

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NON PATENT LITERATURE DOCUMENTS

*Examiner Initial	Cite No.	(Including name of author in capital letters, title of article, title of item, date, pertinent pages, volume-issue number(s), publisher, city and/or country where published.)
	AA	Guiterrez G. et al, "2.488 Gb/s Silicon Bipolar Clock and Data Recovery IC for SONET (OC-48)," IEEE 1998 Custom Integrated Circuits Conference, pp. 575-578.
	AB	Guiterrez, G. and Kong, S., "Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC," VIII-7, 1998 IEEE Radio Frequency Integrated Circuits Symposium, pp. 173-176.
	AC	Hogge, Charles R., Jr., "A Self Correcting Clock Recovery Circuit," IEEE Journal of Lightwave Technology, Vol. LT-3, Dec. 1985, pp. 1312-1314, re-printed as pp. 249-251.
	AD	Hu, T. H. and Gray, P. R., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- μ m CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, Dec. 1993, pp. 1314-1320.
	AE	Jarman, David, "A Brief Introduction to Sigma Delta Conversion," Application Note AN9504, Intersil Corporation, May 1995, pp. 1-7.
	AF	Kawai, K. et al., "A 557-mW, 2.5-Gbit/s SONET/SDH Regenerator-Section Terminating LSI Chip Using Low-Power Bipolar-LSI Design," IEEE Journal of Solid-State Circuits, Vol. 34, No. 1, Jan. 1999, pp. 12-17.
	AG	Lee, T. H. and Bulzacchelli, J. F., "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," IEEE Journal of Solid-State Circuits, Vol. SC-27, Dec. 1992, pp. 1736-1746, re-printed as pp. 421-430.
	AH	Lee, T. H. et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, Dec. 1994, pp. 1491-1496.
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	AJ	Perrott, M. et al., "A 27mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation," IEEE Journal of Solid-States Circuits, Vol. 32, No. 12, Dec. 1997, pp. 2048-2060.
	AK	Pottbacher, A. et al., "A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, Dec. 1992, pp. 1747-1751.
	AL	Razavi, Behzad, "Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits--A Tutorial," Monolithic Phase-Locked Loops and Clock Recovery Circuits--Theory and Design, ed. B. Razavi, IEEE Press, N.Y., 1996, pp. 1-39.
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	AN	Walker, R. C. et al., "A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission," IEEE Journal on Selected Areas in Communications, Vol. 9, No. 5, June 1991, pp. 698-703.
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*Examiner Initial		Document Number	Date	Name
	AA	3,968,493	Jul. 6, 1976	Last et al.
	AB	4,237,423	Dec. 2, 1980	Rhodes
	AC	5,559,841	Sep 24, 1996	Pandula
	AD	6,125,158	Sep. 26, 2000	Carson et al.
	AE	6,151,152	Nov. 21, 2000	Neary
	AF	6,208,211 B1	Mar. 27, 2001	Zipper et al.
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	AL					
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	AA	4,371,974	Feb. 1, 1983	Dugan
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	AL	EP 0590323 A1	April 6, 1994	EP		
	AM	JP 62-81813	April 15, 1987	JP		
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AR	Masaru Kokubo et al, "FA 15.2: A Fast-Frequency-Switching PLL Synthesizer LSI with a Numerical Phase Comparator," IEEE International Solid-State Circuits Conference, New York, Vol. 38, Feb. 1, 1995, pp. 260-261, 376.
AS	Shayan, Y. R. et al., "All Digital Phase-Locked Loop: Concepts, Design and Applications," IEEE Proceedings-F/Radar and Signal Processing 136, Stevenage, Herts, GB, vol. 136, no. 1, Part F, 1 Feb. 1989, pp. 53-56.
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	AB	6,590,426 B2	July 8, 2003	Perrott
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	AD	6,208,211	03-2001	Zipper et al.
	AE	5,495,512	02-1996	Kovacs et al.
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